CLASS-A GaAs FET POWER AMPLIFIER DESIGN FOR OPTIMIZING INTERMODULATION PRODUCT

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ABSTRACT

Since optimizations of amplifier gain and cutoff frequency f of FET are important to minimize nonlinear distortion, intermodulation products of Class-A GaAs FET amplifier is extensively estimated. Output back-off and power added efficiency at any specified D/U ratio are determined under various matching condition using FET's with different f_T .

For optimum design of the amplifier, new charts are given which show the back-off and efficiency at the specified D/U ratio as functions of small-signal gain and ratio of operating frequency to f_T .

1. INTRODUCTION

Improvement of GaAs FET have promoted research and development of various applications of FET amplifiers such as low-noise[1], or broad-band amplifiers[2]. Since recent trend for the MMIC amplifier requires more accurate design, nonlinear distortions of the amplifiers are widely examined, both theoretically and experimentally. Intermodulation products (IMP) which is a measure of nonlinear distortion is investigated extensively [3]-[5]. For example, authors of above papers have reported optimization of load impedance to minimize IMP [3] and reduction of IMP by shorting second harmonic voltage [4]. Most of foregoing papers have adopted figures which show IMP as a function of input level. "Is this expression of IMP the best figure by which a circuit designer can determine optimum condition of the FET amplifier?" Generally speaking, requirement of a microwave transmission system specifies (a) D/U ratio of the nonlinear distortion, (b) output level (c) efficiency, etc. Thus, alternative expression is to show back-off corresponding to the specified D/U ratio as a function of amplifier parameters, such as small signal gain, f_T , etc. Examples of this approach have been shown by G. M. Lambrianou, et. al.[3] whose paper shows constant D/U ratio curves on the impedance plane. However, selection of f_T is also an important factor because the ratio of operating frequency f to f_T affects AM-PM conversion. Thus, optimization of IMP should be done by considering small-signal gain, load impedance and f/f_T as amplifier parameters. This paper describes the optimization of IMP for small-signal gain and f/f_T ratio. The results will be shown graphically in section 3.

2. ESTIMATION METHOD

2.1 Circuit Configuration Assumed in Theoretical Estimation

A series resonance type matching networks are assumed at both input and output of FET, as shown in Fig.1 [6]. Drain source current Ids, gate source capacitance Cgs and gate-source current Igs are assumed as nonlinear elements. Equivalent circuit of an FET is shown in Fig. 2 and parameters in the equivalent circuit are summarized in table 1. Though there is optimum load impedance [3] among those which give the same gain, this paper assumes source and load impedances which cancel imaginary parts of input and output impedances of the FET. This matching condition is selected to reduce frequency dependence of IMP within the amplifier band.

2.2 Calculation Method of Intermodulation Products

Usually intermodulation product is calculated as the response of the amplifier for the input signal with two equal level tones. Thus, the input signal can be regarded as a kind of AM signal of which envelope changes with beat frequency of two tones. If frequency separation between two tones is assumed much smaller than bandwidth of the amplifier, the response of amplifier is very close that for single tone with level equal to the instantaneous level of varying amplitude. The assumption is very convenient to estimate intermodulation products, extensively, for various circuit conditions, because intermodulation product can be calculated by expanding output signal of the amplifier with power series of the input signal. The output voltage signal of the amplifier for single tone is calculated by harmonic balance technique [5] as the function of input level. Both AM-AM and AM-PM conversions are included in the calculated output voltage signal. Thus obtained output voltage is expanded with the power series of the input voltage and intermodulation product is calculated.

3. CALCULATED RESULTS OF INTERMODULATION PRODUCT

Figure 3 shows an example of calculated IMP as a function of input level. Small signal gain is 10 dB and ratio of frequency f to f_T is 0.5. Output level is normalized by 1 dB gain compression level for single tone input. Since IMP higher than 3rd are undesired, D/U ratio is defined as shown in this figure. Dependence of D/U ratio on input level is calculated for various gain and f/f_T ratio and output levels corresponding to the specified D/U ratio are calculated. Results are shown in Fig. 4 which shows output back-off as functions of small signal gain using f/f_T as a parameter. Since input level varies as the function of time with beat frequency of two tone, back-off is defined as the ratio of 1 dB gain compression level to peak output level. Average efficiency over one period of beat frequency is also calculated at the back-off and results are shown in Fig. 5.

Figures 6 and 7 show back-off and efficiency as the function of f/f_T using the specified D/U and small signal gain as parameters. Since optimum small signal gain and f/f_T ratio are determined by Figs. from 4 to 7, these figures give very important information to the amplifier design.

4. CONCLUSION

Intermodulation product of an class-A amplifier was estimated extensively, using harmonic balance technique. Output back-off was calculated as a function of small signal gain and ratio of frequency f to cutoff frequency f_T of FET, using specified D/U ratio as a parameter. Power added efficiency at the back-off was also calculated. These results enable us to determine optimum small signal gain and f/f_T ratio.

5. REFERENCES

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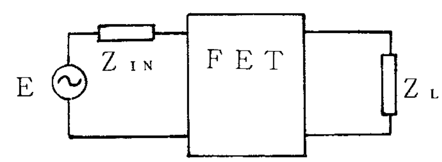

Fig.1 Configuration of amplifier used in the estimation

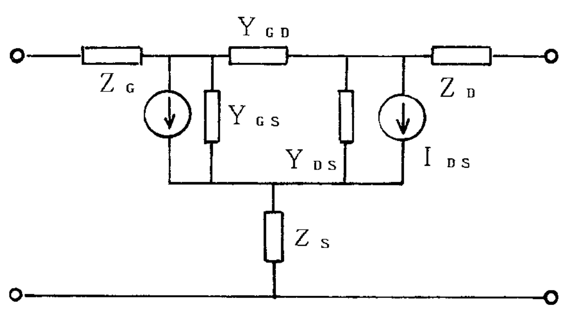

Fig.2 Equivalent circuit of FET

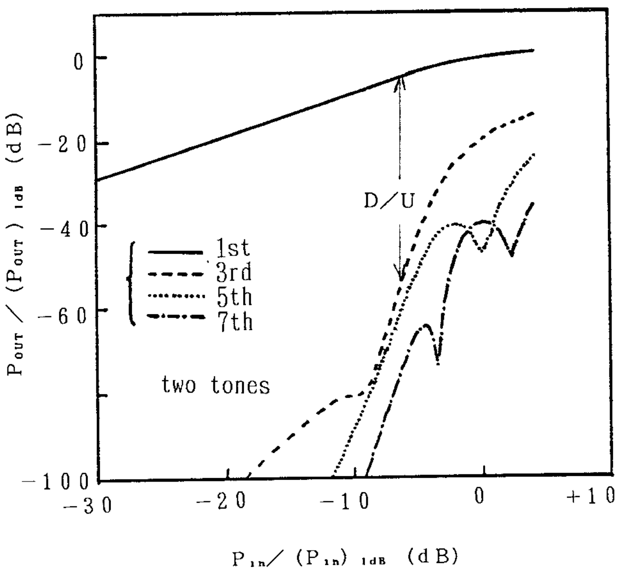

Fig. 3 Intermodulation product vs. input level

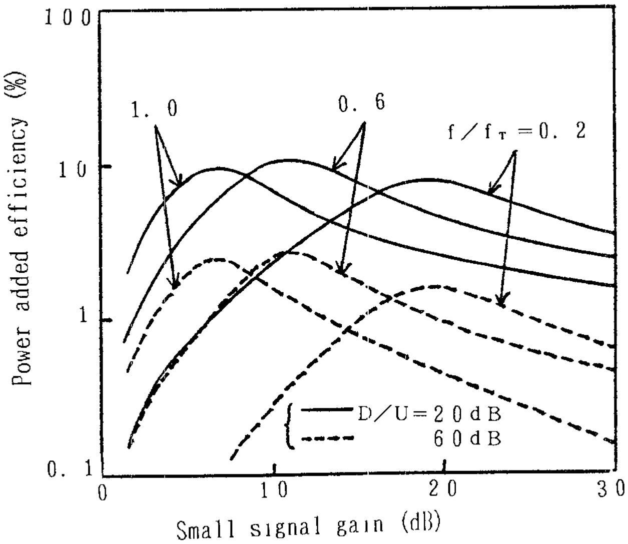

Fig. 5 Power added efficiency at the back-off corresponding to the specified D/U

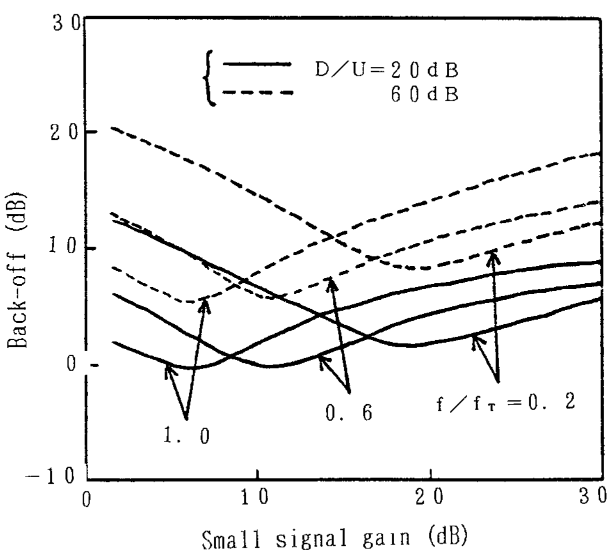

Fig. 4 Required back-off for specified D/U ratio

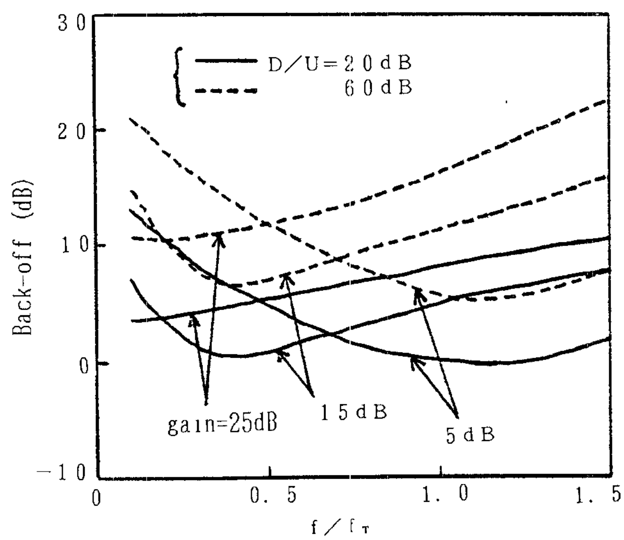

Fig. 6 Back-off vs. f/f_T

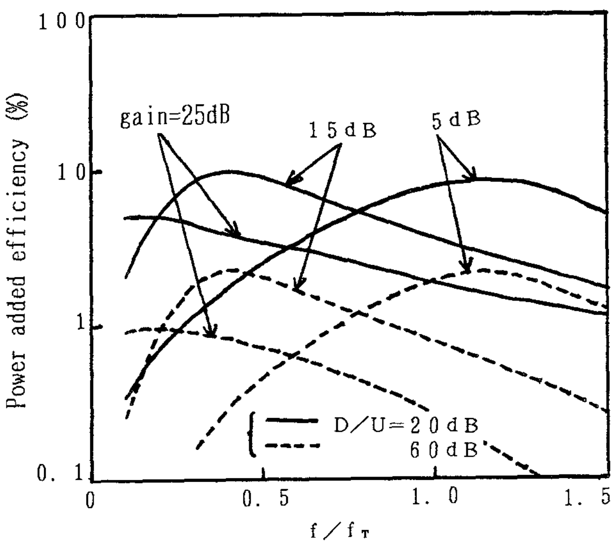

Fig.7 Power added eficiency vs f/f_T

Table 1 Parameter values of FET equivalent circuit

parasitic elements	r_D	0.609Ω
	r_G	0.258Ω
	r_S	0.609Ω
	L_D	0.01nH
	L_G	0.03nH
	L_S	0.003nH
intrinsic capacity	C_{GS} (0)	0.706pF
	C_{GD}	0.127pF
	C_{DS}	0.010pF
drain current	β	9.9×10^{-4}
	γ	2.006
	a_0	0.0411
	a_1	0.0795
	a_2	0.0583
	a_3	0.0334
	V_{DSO}	3.0